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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Modulation code system and methods for encoding and decoding a signal

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Modulation code system and methods for encoding and decoding a signal

The invention relates to a modulation code system as shown in figure 6, including an encoder 100 for transforming an original signal s into an encoded signal c satisfying predefined second constraints before being transmitted via a channel 300 or stored on a recording medium (not shown). That modulation code system further comprises a decoder 200 for decoding the encoded signal c after restoration or receipt back into the original signal s. The invention further relates to a decoder, encoder, signal and record carrier. Furthermore the invention relates to a method for encoding and decoding.

Such a modulated code system known in the art is substantially used in data transmission systems or data storage systems.

The invention further relates to known methods for operating the encoder 100 and the decoder 200.

Hereinafter different signals are referred to, satisfying different constraints, respectively. The constraints are typically either simple or complicated. A signal satisfying simple constraints is e.g. a (0,k)-constrained signal, which is a binary signal where the number of consecutive zeros is at most k+1. To the contrary, a signal satisfying complicated constraints is a signal obeying run length constraints on more complicated patterns, like e.g. the transition patterns of the anti-whistle patterns as listed in table 1.

Traditionally, encoders or decoders of modulation code systems use specific modulation methods, e.g. the enumerative encoding method or the integrated scrambling method. The enumerative encoding method is e.g. known from K.A.S. Immink, "A practical method for approaching the channel capacity of constrained channels", IEEE Trans. Inform. Theory, vol. IT-43, no. 5, pp.1389-1399, Sept. 1997. The integrated scrambling method is e.g. known from K.A.S. Immink, "Codes for mass data storage systems", Shannon Foundation Publishers, The Netherlands, 1999.

Modulation codes such as (d,k)-codes and (d,k)-RLL codes are widely employed in digital transmission and storage systems. A modulation code consists of an encoder which servers to transform arbitrary sequences of source bits into sequences that obey certain constraints and a decoder to recover the original source from the constrained sequence. A binary sequence is said to be (d,k)-constrained if any two consecutive ones in

the sequence are separated by at least d and at most k zeroes; it is said to be (d,k)-RLL constrained if the minimum and maximum run lengths are at least d+1 and at most k+1, respectively. The use of constrained sequences enable the data receiver to extract control information to be used for example timing recovery, gain control, or equalisation adaptation.

Many modern data receivers employ adaptive equalization or bandwidth control. In some CD or DVD systems two-dimensional adaptive equalization is used to combat not only inter-symbol interference along the track but also inter-track interference (cross-talk cancellation). Also, in certain data receivers the only adaptive part is a circuit for slope control. In order for such systems to function properly, the frequency components of the received signal must obey certain constraints which in turn dictates the use of data sequences in which the maximum (run)length of certain (periodic) data patterns are limited. As a typical example are mentioned constraints on data patterns of period 1 or 2 (k_1- and k_2-constraints) that are already used in practical systems. Periodic data patterns with a specific length will result in a whistle with a respective frequency. A known problem in receiving systems is that whistles in a received signal has a negative influence on the functioning of for example the PLL's in the receiver or gain control and thus the reconstruction of the transmitted data. Therefore, there is a need to generate data sequences that do not generate sequences that could negatively influence on the reconstruction of the transmitted data .

Hereafter some definitions are given to improve the understanding of the technical field.

A sequence is $(k;\mathbf{p})$-pattern-constrained if it does not contain a run of length k of the pattern $\mathbf{p}$. Given a pattern $\mathbf{p} = (p_0\, p_1 \ldots p_{e-1}\, p_e)$ which is interpreted as representing the periodic sequence $\ldots, p_0, p_1, \ldots, p_{e-1}, p_e, p_0, p_1, \ldots, p_{e-1}, \ldots$ of period e. A sequence is $(\mathbf{k};\mathrm{P})$-pattern constrained if the sequence is $(k_i,\mathbf{p}^{(i)})$-constrained for all i, wherein $\mathbf{k} = k_1,\ldots, k_i,$ which is a sequence of positive integers k, and $\mathrm{P} = ,\mathbf{p}^{(1)},\ldots, ,\mathbf{p}^{(i)}$, which is a sequence of periodic patterns. A sequence is P-pattern-constrained if it is $(\mathbf{k};\mathrm{P})$-pattern constrained for some $\mathbf{k}$.

A k-constraint sequence is a binary sequence where the number of consecutive zeroes is at most k. These sequences are precisely the $(k;\mathbf{p})$-constrained sequences for the pattern $\mathbf{p} = (0)$.

A k-RLL-constrained sequence is a sequence with symbols from {-1,1}, thus a binary sequence, where the maximum run of each of the symbols is at most k+1. These sequences are precisely the $(\mathbf{k};\mathrm{P})$-pattern constrained sequences with $\mathbf{k} = k$+1 and $\mathrm{P} = (-1)$, (1).

An anti-whistle constrained sequence is a pattern that has only a single frequency component in the pass band ranging from dc to the Nyquist frequency. Table 1 discloses some anti-whistle patterns and the corresponding index. Anti-whistle transition patterns are obtained by one time integrating/differentiating the anti-whistle pattern.

index	anti-whistle pattern	period anti-whistle pattern	anti-whistle transition pattern	period anti-whistle transition pattern
1	0	1	0	1
2	01	2	1	1
4^a	0011	4	01	2
4^b	0111	4	0011	4
3	011	3	011	3
6	000111	6	001	3

Table 1: Anti-whistle transition patterns.

These known methods of encoding/decoding enable the transformation of the original signal s into the signal c satisfying second constraints and back, usually at a modulation code rate close to 1. The rate of a modulation code is a number that refers to the average number of encoded signals per source symbol: For example, an encoder of rate 1/2 code produces (on average) two encoded symbols for each source symbol.

At least the decoder of such known modulation code systems is usually implemented in hardware for enabling high-speed operation. However, hardware implementation of the above mentioned modulation code methods disadvantageously requires quite a lot of hardware, e.g. to store necessary tables. In the known modulation coders the relation between input words and corresponding output words is uniquely defined.

Starting from that prior art it is the object of the invention to improve a known modulation code system, an encoder and a decoder as well as known methods for operating the encoder and the decoder such that their implementations require less hardware.

A modulation code system according to the invention comprises

- a modulation code encoder (110) for coding the original signal s into an intermediate signal t satisfying predefined first constraints;
- a transformer encoder (120) for converting said intermediate signal t in order to generate an encoded signal c satisfying a predefined second constraint

- means for supplying the encoded signal c to a medium;
- means for retrieving the encoded signal c from said medium;
- a transformer decoder (220) for converting the encoded signal c so as to obtain said intermediate signal t and
- a modulation code decoder (210) for decoding said intermediate signal t into said original signal s

wherein the transformer decoder (220) is adapted to convert a signal that violates the predefined second constraint into another signal that violates the predefined first constraint, the transformer decoder (220) having a polynomial function b(D), and that the transformer encoder (120) has the polynomial function 1/b(D).

The invention is based on the following recognition. The first constraints of the modulation code encoder may in general be simpler, equal or more complicated than the second constraints of the channel signal. However, in typical applications the first constraints are simpler than the second constraints. The signals that violate the second constraint are the signals that have a negative influence on the functioning of a receiver or playback apparatus. As a lot of effort is done to make the known encoders that generate the first constraint signal, it will take even more effort to adapt the encoders to make them to comply with more complicated constraints, such as anti-whistle constraints. Normally, only a limited number of periodic signals have a negative influence on the functioning of PLL's or other control/servo circuits in a receiver or playback apparatus, these periodic signals will be referred to as forbidden signals. These forbidden signals should therefore not be generated and transmitted by the modulation code system. Furthermore, as the known encoder is arranged to generate constraint signals such as (0,k)-constrained signal, said encoders will not generate a lot of patterns, namely the patterns that does not comply with the constraint. The number of patterns that does not comply with the constraint, and that will not be generated by the known encoders, is larger than the number of periodic signals that should not be generated. The transformer decoder is designed such that it transforms forbidden signals into signals that do not comply with the constraints of the encoder. Assume that the transformer decoder has the polynomial function b(D). By determining the inverse function of the transformer decoder the polynomial function of the transformer encoder 1/b(D) can be determined. Said transformer encoder transforms signals that does not comply with the constraints of the modulation code encoder into the forbidden signals. In normal operation the modulation code encoder will not generate signals that does not comply with the constraints of the modulation code encoder and therefore the transformer encoder according

to the invention will not generate the forbidden signals. In a preferred embodiment the polynomial function b(D) is a linear polynomial function.

The claimed design of the modulation code system, in particular the series connection of the modulation code encoder with the transformer encoder within said encoder and the series connection of the transformer decoder with said modulation code decoder within said decoder, ensures that the hardware expense for implementing the encoder and the decoder is advantageously essentially reduced with making use of the benefits of the characteristics of the known modulation coders.

In a preferred embodiment of the invention, the predefined first constraint is a k-constraint and the predefined second constraint is at least an anti-whistle-constraint. Preferably the transformer encoder and transformer decoder are in the form of a linear feedback filter and linear filter, respectively. This type of filters can be easily implemented in hardware as well in software. The invention can be used in any kind of transmission or recording system, which makes use of known modulation coding system.

In a preferred embodiment of the invention, the modulation code encoder/decoder is a (0,k)-encoder; in that case the intermediate sequence t is (0,k)-constrained and thus satisfies a very simple constraint.

Further advantageous embodiments of both, the encoder and the decoder are subject matter of the dependent claims.

Six figures are accompanying the description, wherein

Figure 1 shows a modulation code system according to the present invention;

Figure 2 shows a transformer encoder according to the present invention;

Figure 3 shows a transformer decoder according to the present invention;

Figure 4 shows a flow chart illustrating the operation of an encoder according to the present invention;

Figure 5 shows a flow chart illustrating the operation of a decoder according to the present invention; and

Figure 6 shows a modulation code system known in the art.

In the following a preferred embodiment of the modulation code system according to the invention will be described in more detail by referring to figures 1 to 5.

At first the design of said modulation code system, in particular the design of the linear shift register 120 and of the sliding block decoder filter 220, will be described by referring to figures 1 to 3.

Figure 1 illustrates the design of the modulation code system. It comprises an encoder 100 for transforming an original signal s into an encoded signal c satisfying predefined second constraints, such as anti-whistle constraints. Said encoder 100 includes a series connection of a modulation code encoder 110 receiving said original signal s and a transformer encoder 120 for outputting said encoded signal c.

Said encoded signal c is e.g. transmitted via a channel 300 or stored on a recording medium (not shown). Any suitable recording medium can be used such as Hard disk drive, optical disc, and flash memory.

After transmission via said channel 300 or after being restored from said recording medium the encoded signal c is input to a decoder 200 of said modulation code system in order to re-generate said original signal s. For achieving this, the decoder 200 comprises a transformer decoder 220 for receiving said transmitted or restored encoded signal c and a modulation code decoder 210 being connected in series behind said sliding block decoder filter 200 in order to output said desired original signal s.

Figure 2 shows a preferred embodiment of the transformer encoder 120 comprising a linear shift register. The linear shift register is represented by N delay elements 120-1, …, 120-N each of which may be embodied as flip-flop. The delay elements 120-1, ... 120-N are connected in series such that e.g. the bits c_{j-1}-$c_{j-(N-1)}$ simultaneously output by said delay elements 120-1 to 120-(N-1), respectively are input to the respective consecutive delay elements 120-2 to 120-N, respectively. Moreover, said transformer encoder 120 comprises N multiplier elements 121-1, ... 121-N each of which receiving another one of said N bits c_{j-1}-c_{j-N} output of said delay elements 122-1, ... 122-N, respectively and multiplying the received bits c_{j-1}-c_{j-N} with a constant m_1, ... m_N, respectively, for generating N multiplier output signals. Said transformer encoder 120 further comprises a first XOR-gate 122 for receiving and XOR-combining said N multiplier output signals in order to generate a first XOR-output signal. Said first XOR-output signal is XOR-combined by a second XOR-gate 123 with bits t_j of a received intermediate signal t output by said modulation code encoder 110. Said intermediate signal t might be latched in a memory (not shown) before being input to said transformer encoder 120. At its output said second XOR-gate 123 generates a second XOR-output signal representing the encoded signal c output by

said transformer encoder 120. Said encoded signal c is bit wise, i.e. bits c_j thereof are, input into the first delay element 121-1 of said linear shift register 120-1, ... 120-N.

The transformer encoder 120 is preferably embodied in hardware in order to enable high operation speed.

Figure 3 shows a sliding block decoder representing a preferred embodiment of the transformer decoder 220. In said embodiment the transformer decoder 220 comprises a linear shift register being represented by N delay elements 220-1, …, 220-N each of which may be embodied as flip-flop. N being an integer greater than 2. The delay elements 220-1, ... 220-N are connected in series such that e.g. the output bits c_{j-1}-$c_{j-(N-1)}$ of said delay elements 220-1 to 220-(N-1) are input to the respective consecutive delay elements 220-2 to 220-N, respectively. Moreover, said transformer decoder 220 comprises N multiplier elements 221-1, ... 221-N each of which receiving another one of said N bits c_{j-1}-c_{j-N} output of said delay elements 222-1, ... 222-N, respectively and multiplying the received bits c_{j-1}-c_{j-N} with a constant b_1, ... b_N, respectively, for generating N multiplier output signals. Said transformer decoder 220 further comprises a XOR-gate 222 for receiving and XOR-combining said N multiplier output signals in order to regenerate the intermediate signal t having bits tj.

Said transformer decoder 220 is preferably implemented in hardware in order to enable a high operation speed.

The intermediate signal t output by said transformer decoder 220 might be latched in a memory (not shown) before being input to said modulation code decoder 210.

In the following the operation of the encoder 100 and of the decoder 200 will be explained in more detail by referring to figures 4 and 5.

In figure 4 the operation of the modulation code encoder 110 and of the transformer encoder 120 are explained in more detail. More specifically, the modulation code encoder 110 receives the original input signal s the source bits s_j of which are grouped into blocks s_{np}, s_{np+1}, ..., $s_{(n+1)p-1}$ of p bits, respectively (see method step S4-1).

Subsequently, these blocks are - according to method step S4-2 - encoded into a code word block t_{nq} ... $t_{(n+1)q-1}$ of q bits, respectively. Said encoding is done in the encoder 110 using in order to generate the intermediate signal t by using a predetermined modulation code.

Said intermediate signal t is subsequently recursively filtered by said linear feedback shift register 120 in order to generate the encoded signal c. More specifically, in said shift register 120 each bit c_j of said encoded signal c is generated from a bit t_j of said

intermediate signal t and of previously computed bits c_{j-n} according to the following recursive equation:

$$c_j = t_j \oplus m_1.c_{j-1} \oplus \ldots \oplus m_N.c_{jN,} \qquad (1)$$

wherein $\oplus$ indicates an XOR-operation in the case of binary signals and N being an integer preferably larger than 3.

Formula (1) represents the XOR-combination done by the first and the second XOR-gate 122, 123 as shown in Fig. 2 (method step S4-3).

Subsequently, the thus generated encoded signal c representing a sequence of said bits c_j is output to a channel 300 according to method step S4-4.

Figure 5 illustrates the operation of the decoder 200. More specifically, according to method step S5-1 the sliding block decoder filter 220 sequentially receives the bits c_j of the encoded signal c after transmission or after restoration from the recording medium. In said sliding block decoder filter 220 the intermediate signal t is in step S5-1 bit wise restored by computing the respective bits t_j of said intermediate signal t according to the following equation:

$$t_j = c_j \oplus b_1.c_{j-1} \oplus \ldots \oplus b_N.c_{j-N.} \qquad (2)$$

Said formula (2) represents the operation of the XOR-gate 222 as shown in Fig. 3.

Moreover, in said sliding block decoder the bits of said intermediate signal t_j^0 are - according to method step S5-2 - grouped into blocks $t_{nq} \ldots t_{(n+1)q-1}$ of q bits, respectively.

Finally, said blocks are decoded according to method step S5-3 into a source word $s_{np}, \ldots, s_{n+1,p-1}$ of the original signal s. This decoding step S5-5 is done by using the modulation code decoder 210 of a predetermined modulation code.

It should be noted that the step S4-2 performs the encoding by a known modulation encoder and the step S5-3 performs the decoding by a known modulation decoder.

In the following mathematical background information is given about an appropriate design of the linear feedback shift register 120 and of the sliding block decoder filter 220 according to the invention. Hereinafter, the signals s,t and c are referred to as sequences s,t and c, respectively.

First a mathematical description is given of the transformer encoder 120 and the corresponding transformer decoder 220 as shown in Fig. 2 and Fig. 3.

Let F be a field (typically F = GF(2)). The finite field GF(2) consists of elements 0 and 1 which satisfy the following addition and multiplication rules:

$0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, 1 + 1 = 0,$

$0 \times 0 = 0, 0 \times 1 = 0, 1 \times 0 = 0, 1 \times 1 = 1.$

Consider a sliding block decoder filter map ϕ of the form

$$\phi(c_0, \ldots, c_N) = \sum_{n=0}^{N} b_n c_{N-n}. \tag{3}$$

Of course, we may assume without loss of generality that

$$b_0 \neq 0. \tag{4}$$

With such a map, we associate its window polynomial

$$b(D) = \sum_{n=0}^{N} b_n D^n$$

in the delay operator D. With each sequence c over F, we associate the formal power series

$$c(D) = \sum_j c_j D^j .$$

Now if the sequence t is the image of the sequence c under the block map ϕ, then

$$t_j = \phi(c_{j-N}, \ldots c_j) = \sum_{n=0}^{N} b_n c_{j-n} \tag{5}$$

so that t is the result of the convolution of c with b, that is,

$$t(D) = c(D)b(D).$$

Note that due to the condition (4), such a block map is indeed invertible. Indeed, if a sequence t is encoded into the sequence c by letting

$$c_j = (t_{j+s} - \sum_{n=1}^{N} b_n c_{j-n}) / b_0, \tag{6}$$

then c is decoded to t by the sliding block decoder with block map as in (5). From (6) it can be seen that the encoding operation is in fact linear feedback filtering with polynomial function 1/b(D). Where the decoding operation is a linear filter with polynomial function b(D).

Let $p = (p_0 \ldots p_{e-1})$. The sequence c will be said to be (k;p)-pattern-constrained if no block of k+1 consecutive symbols from c is equal to one of the e blocks $p_i p_{i+1} \ldots p_{i+k}$, $i = 0, \ldots, e-1$ (read indices modulo e if $k \geq e$). Now the next problem is how to design the transformer encoder 120 and the transformer decoder 220, that is, how to choose the window

polynomial b(D), so that the sequence c in Fig. 1 satisfies a (k';p)-pattern constraint for some k'.

First, supposing that the simple constraint is a (0,k)-constraint, that is, supposing that the modulation code encoder 110 outputs a sequence t that is known not to contain a run of k+1 consecutive zeroes.

With the periodic pattern $p=(p_0 \ldots p_{e-1})$, the pattern polynomial

$$p(D) = \sum_{i=0}^{e-1} p_i D^i$$

is associated.

Supposing that the "window" of the sliding block decoder is entirely filled with the periodic pattern, that is, supposing that in equation (5), it is the case that $c_j = p_{j+r \bmod e}$, $j = n-N, \ldots, n$, for some integer r. Then t_j is the (j+r mod e)'th coefficient of the polynomial $b(D)p(D) \bmod D^e-1$. From that it follows:

Lemma 1: The image of a pattern $p = (p_0 \ldots p_{e-1})$ under the block map with associated window polynomial b(D) is the zero-pattern if and only if $p(D)b(D) = 0 \bmod D^e-1$, that is, if and only if b(D) is divisible by the polynomial

$$b_p(D) := (D^e - 1)/\gcd(D^e-1, p(D)).$$

The function gcd is the function that determines the greatest common divisible of the corresponding polynomials.

The polynomial $b_p(D)$ in the above lemma will hereinafter be referred to as the (minimal) annihilator polynomial associated with the pattern p. As a consequence of Lemma 1, there follows:

Theorem 2: Let $P = (p^{(1)}, \ldots p^{(r)})$denote a collection of periodic patterns. Let the polynomial $b_p(D)$ be defined as the least common multiple (lcm) of the minimal annihilator polynomials of the patterns in P, that is,

$$b_P(D) := lcm\left\{ b_{p^{(i)}}(D) \mid i=1,\ldots,r \right\}.$$

Then all the periodic patterns from P are mapped onto the zero pattern under a block map with associated window polynomial b(D) if and only if b(D) is divisible by $b_p(D)$.

Corollary 1: The modulation code obtained as the concatenation of a k-constrained code and the rate-1 code obtained from an invertible linear block map with window polynomial b(D) satisfies a p-pattern-constraint if and only if $b_p(D)$ divides b(D). If that is the case, then it satisfies a (k+N,p)-pattern-constraint, where d denotes the degree of b(D).

The construction method implicit in Corollary 1 represents what in the whole specification is referred to as the recursive filtering method.

Example 1. The recursive filtering method shall in this example be used to design a code for the anti-whistle constraints (see Table 2). It is worked over the GF(2). In Table 2 there are listed the binary anti-whistle patterns p, the associated window polynomials p(D), and the minimal annihilators $b_p(D)$ over GF(2). (There are listed all polarities for each pattern.) To check the entries in this table, note that since all computations are modulo 2, we have that

$$D^2-1 \equiv (1+D)^2;$$
$$D^3-1 \equiv (1+D)(1+D+D^2);$$
$$D^4-1 \equiv (1+D)^4.$$
$$D^6-1 \equiv (D^3+1)^2 \equiv (1+D)^2 (1+D+D^2)^2$$

index	binary pattern	period	pattern polynomial	minimal annihilator
1(0)	0	1	0	1
1(1)	1	1	1	1+D
2	01	2	1	$(1+D)^2$
4^a	0011	4	1+D	$(1+D)^3$
$4^b(0)$	1000	4	1	$(1+D)^4$
$4^b(1)$	0111	4	$1+D+D^2$	$(1+D)^4$
3(0)	100	3	1	$(1+D)(1+D+D^2)$
3(1)	011	3	1+D	$1+D+D^2$
6	000111	6	$1+D+D^2$	$(1+D)^2(1+D+D^2)$

Table 2: Anti-whistle patterns with associated polynomials and annihilators.

It can immediately be seen from Table 2 that the annihilator polynomial $b_p(D)$ for the collection P of anti-whistle patterns equals

$$b_p(D) = (1+D)^4 (1+D+D^2) \equiv 1+D+D^2+D^4+D^5+D^6. \qquad (7)$$

So the recursive filter with polynomial function $1/b_p(D)$ transforms a k-constrained sequence into an anti-whistle constrained sequence where the run length of each anti-whistle pattern is at most k+6.

Finally, in order to investigate the efficiency of the method, the full set of patterns annihilated by the anti-whistle polynomial $b_p(D)$ in (7) shall be determined. Since both the polynomials

$$D^4\text{-}1 \equiv (1+D)^4, \quad D^3\text{-}1 \equiv (1+D)(1+D+D^2)$$

divide the anti-whistle polynomial, it annihilates all patterns of period three and four. Also, since $D^{12}\text{-}1 \equiv (D^3\text{-}1)^4 \equiv (1+D)^4 (1+D+D^2)^4$ is divisible by the anti-whistle polynomial, each annihilated pattern is also annihilated by $D^{12}\text{-}1$, hence necessarily has period 12. Now if p is a pattern of period 12, then it is annihilated by the anti-whistle polynomial if and only if the associated pattern polynomial p(D) satisfies

$$p(D)b_p(D) \equiv 0 \bmod D^{12}\text{-}1$$

over GF(2), which is the case if and only if

$$p(D) \equiv 0 \bmod (1+D+D^2)^3.$$

If in fact p has a period smaller than 12, then it has period 4 (so is annihilated) or period 6. By a similar reasoning as before, a pattern of period 6 is annihilated if and only if its associated pattern polynomial p(D) satisfies $p(D) \equiv 0 \bmod 1+D+D^{2.}$

It is now an easy exercise to determine all patterns that are annihilated by the anti-whistle polynomial. The following remark will further reduce the computations. In general, a pattern p of period e has in fact a smaller period e′, for some divisor e′ of e, if and only if its associated pattern polynomial p(D) is divisible by $(D^e\text{-}1)/(D^{e'}\text{-}1) = 1+D^{e'} + \dots + D^{(q-1)e'}$, where q = e/e′. For example, a pattern of smallest period 6 that is annihilated by the anti-whistle polynomial has an associated pattern polynomial of the form $p(D) = (1+D+D^2)a(D)$ with a(D) of degree at most 5 and not divisible by 1+D or by $1+D+D^2$. Using this, it can be seen that the only patterns annihilated by the anti-whistle polynomial are the anti-whistle patterns together with some patterns of smallest period 12.

So in this case only a few additional, very weak constraints are introduced by the transformation coding and hence the efficiency of the overall modulation code almost equals the efficiency of the overall modulation code encoder 110 on which the overall code is based. Therefore, the invention is very suitable to be used with known encoders and decoders which has a modulation code rate close to 1, as it is very difficult to add new constraints to said known encoders and decoders

More general, supposing that the simple constraint is a (k,a)-pattern-constraint, for some pattern $a = (a_0, a_1, \dots, a_{f\text{-}1})$. Then in a simpler way it follows that to get a (k';p)-pattern-constraint for some k', the polynomial b(D) must be chosen so that $p(D)b(D) = a(D) \bmod D^f\text{-}1$.

Though the invention is described with reference to preferred embodiments thereof, it is to be understood that these are non-limitative examples. Thus, various modifications are conceivable to those skilled in the art, without departing from the scope of the invention, as defined by the claims.

The use of the verb "to comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. Furthermore, the use of the article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the claims, any reference signs placed between parentheses shall not be construed as limiting the scope of the claims. The invention may be implemented by means of hardware as well as software. The same item of hardware may represent several "means". Furthermore, the invention resides in each and every novel feature or combination of features.

CLAIMS:

1. Modulation code system comprising

a modulation code encoder (110) for coding the original signal s into an intermediate signal t satisfying predefined first constraints;

a transformer encoder (120) for converting said intermediate signal t in order to generate an encoded signal c satisfying a predefined second constraint

means for supplying the encoded signal c to a medium;

means for retrieving the encoded signal c from said medium;

a transformer decoder (220) for converting the encoded signal c so as to obtain said intermediate signal t and

a modulation code decoder (210) for decoding said intermediate signal t into said original signal s

wherein the transformer decoder (220) is adapted to convert a signal that violates the predefined second constraint into another signal that violates the predefined first constraint, the transformer decoder (220) having a polynomial function b(D), and that the transformer encoder (120) has the polynomial function 1/b(D).

2. The modulation code system as claimed in claim 1, wherein the predefined first constraint is a k-constraint and the predefined second constraint is at least an anti-whistle-constraint.

3. The modulation code system as claimed in claim 1 or 2, wherein the transformer encoder is in the form of a linear feedback filter.

4. The modulation code system as claimed in claim 1 or 2, wherein the transformer encoder is in the form of a linear filter.

5. The modulation code system as claimed in claim 1 or 2, wherein the medium is a record carrier.

6. The modulation code system as claimed in claim 1 or 2, wherein the medium is a transmission medium.

7. A decoder (200) for use in the modulation code system as claimed in claim 1, for retrieving an original signal s from an encoded signal c, the decoder comprising

a transformer decoder (220) for filtering the encoded signal c in order to generate an intermediate signal t ; and

a modulation code decoder (210) for decoding said intermediate signal t into said original signal s, wherein the transformer decoder (220) is adapted to convert a signal that violates a predefined second constraint into another signal that violates a predefined first constraint, the transformer decoder (220) having a polynomial function b(D).

8. The decoder as claimed in claim 7, wherein the predefined first constraint is a k-constraint and the predefined second constraint is at least an anti-whistle-constraint.

9. The decoder as claimed in claim 7 or 8, wherein the transformer decoder is in the form of a linear filter.

10. The decoder (200) according to claim 7 or 8, characterized in that the transformer decoder (220) is embodied as sliding block decoder filter comprising

a linear shift register consisting of N delay elements (220-1,...,220-N) being connected in series wherein the first delay element (220-1) of said series connection receives the encoded signal c after transmission or restoration and wherein the output signals of the first N-1 delay elements (220-1,...,220-(N-1)) are input to the respective consecutive delay elements (220-2,...,220-N);

N multiplier elements (221-1,...,221-N) each of which receiving another one of said N output signals of said delay elements (222-1, ...,222-N) and multiplying the received delay output signal with a given constant ($b_1,...,b_N$) for generating a multiplier output signal, respectively; and

a XOR-gate (222) for receiving and XOR-combining said N multiplier output signals and said encoded signal c in order to generate the intermediate signal t as output by the transformer decoder (220), N being an integer larger than 2.

11. The decoder (200) according to claim 7 or 8, characterized in that the transformer decoder (220) is implemented at least partly in software or hardware.

12. The decoder (200) according to claim 7 or 8, characterized in that the decoder (200) has a modulation code rate close to 1.

13. The decoder (200) according to claim 7 or 8, characterized in that the modulation code decoder (210) is an (0,k)-decoder.

14. Decoding method for decoding an encoded signal c satisfying predetermined second constraints into an original signal; characterized by the following steps:

filtering the encoded signal c by means of the polynomial function 1/b(D), in order to generate an intermediate signal t satisfying predetermined first constraints, wherein b(D) is a polynomial function that converts a signal that violates the predefined second constraints into another signal that violates the predefined first constraints; and

decoding the intermediate signal t into the original signal s .

15. An encoder (100) for use in the modulation code system as claimed in claim 1, wherein the encoder comprises

a modulation code encoder (110) for transforming the original signal s into the intermediate signal t satisfying predefined first constraints; and

the transformer encoder (120) has the polynomial function 1/b(D), for filtering said intermediate signal t in order to generate said encoded signal c satisfying predefined second constraints, wherein b(D) is a polynomial function that converts a signal that violates the predefined second constraints into another signal that violates the predefined first constraints.

16. The encoder as claimed in claim 15, wherein the predefined first constraint is a k-constraint and the predefined second constraint is at least an anti-whistle-constraint.

17. The encoder as claimed in claim 15 or 16, wherein the transformer encoder is in the form of a linear feedback filter.

18. The encoder (100) according to claim 15, characterized in that the transformer encoder (120) comprises

a linear shift register consisting of N delay elements (120-n with n = 1-N) being connected in series such that the output signals of the N-1 delay elements (120-1 to 120-(N-1)) are input to the consecutive delay element (120-2 to 120-N), respectively;

N multiplier elements (121-n) each of which receiving another one of said N output signals of said delay elements (122-1, ..., 122-N) and multiplying the received delay element output signal with a constant (m_1, ... m_N) for generating a multiplier output signal, respectively;

a first XOR-gate (122) for receiving and XOR-combining said N multiplier output signals in order to generate a first XOR-output signal; and

a second XOR-gate (123) for XOR-combining the intermediate signal t output by said modulation code encoder 110 with said first XOR-output signal in order to generate a second XOR-output signal which corresponds to the encoded signal c output by said transformer encoder (120) and which is input to the first delay element (120-1) of said series connection of delay elements (121-1,....,120-N), N being an integer larger than 2.

19. The encoder (100) according to claim 15, characterized in that the transformer encoder (120) is implemented in software or hardware.

20. The encoder according to claim 15, characterized in that the encoder (100) has a modulation code rate close to 1.

21. The encoder according to claim 15, characterized in that the modulation code encoder (110) is an (0,k)-encoder.

22. Encoding method for transforming an original signal s into an encoded signal c satisfying predefined second constraints;
characterized by the following steps:

transforming the original signal s into an intermediate signal t satisfying predefined first constraints; and

filtering the intermediate signal t by means of the polynomial function 1/b(D), in order to generate an encoded signal c satisfying predefined second constraints, wherein

b(D) is a polynomial function that converts a signal that violates the predefined second constraints into another signal that violates the predefined first constraints.

23. Encoded signal obtained with the encoding method according to claim 22.

24. Record carrier carrying the encoded signal obtained with the encoding method according to claim 22.

ABSTRACT:

The invention relates to a modulation code system and a corresponding modulation method. Said modulation system comprises an encoder 100 for transforming an original signal s into an encoded signal c satisfying predefined second constraints. Said modulation code system further comprises a decoder 200 for decoding the encoded signal c after restoration back into the original signal s. It is the object of the invention to improve such a known modulation code system and method in the way that the amount of required hardware is reduced. This object is solved according to the invention by designing the encoder 100 such that it comprises a series connection of a modulation code encoder 110 and of a transformer encoder 120 serving for filtering an intermediate signal t output by said modulation code encoder 110 and satisfying predefined first constraints in order to generate said encoder output signal c. The object is further solved by the decoder 200 comprising a series connection of a transformer decoder 220 and of a modulation code decoder 210.

Figure 1

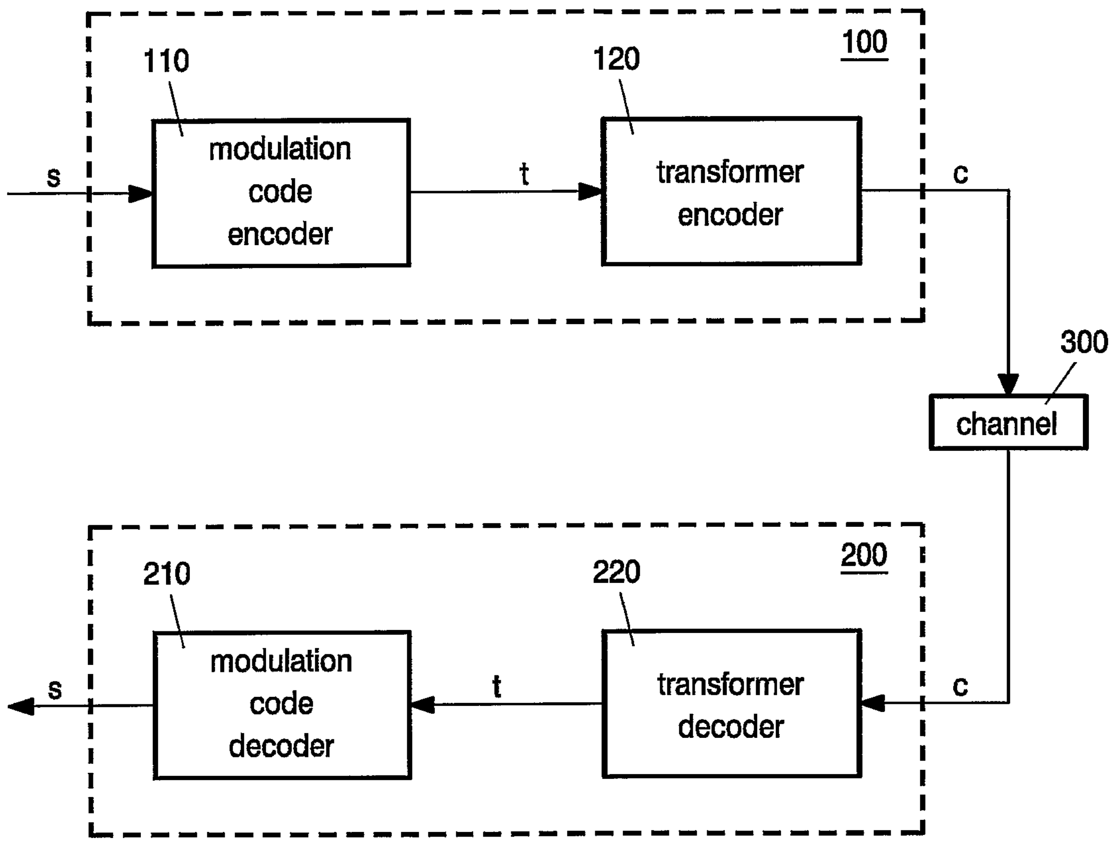
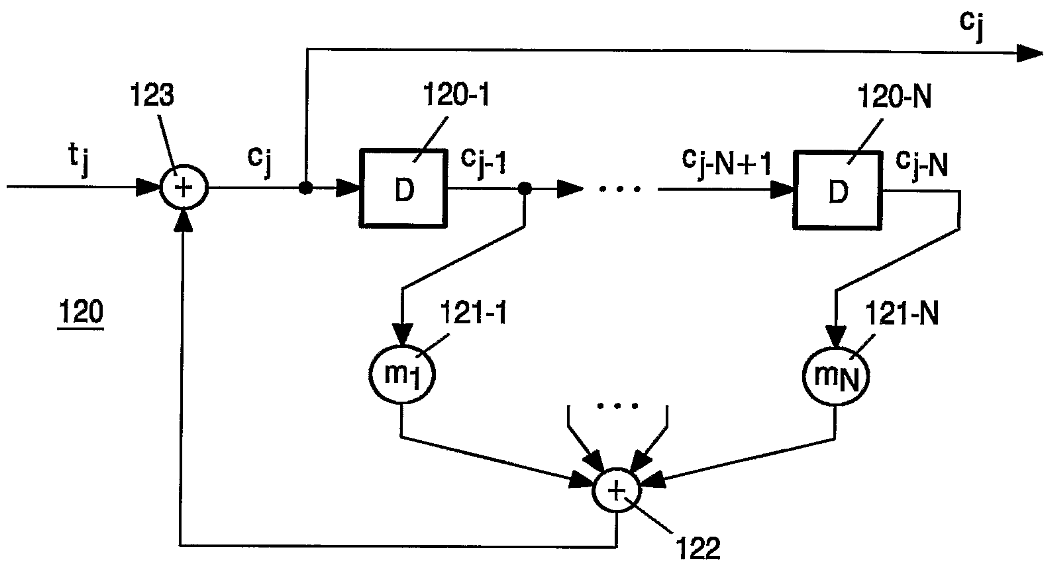
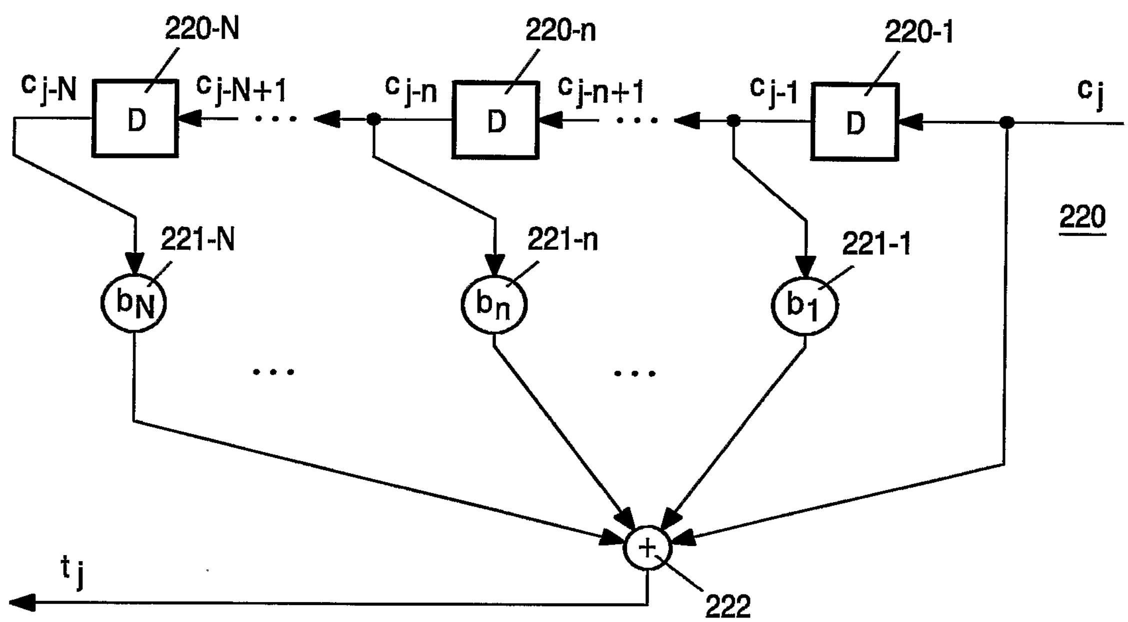

100
110
120
s
modulation code encoder
t
transformer encoder
c
300
channel
200
210
220
s
modulation code decoder
t
transformer decoder
c

FIG. 1



c_j
123
120-1
120-N
t_j
c_j
c_{j-1}
c_{j-N+1}
c_{j-N}
D
D
120
121-1
121-N
m_1
m_N
122

FIG. 2



220-N
220-n
220-1
c_{j-N}
c_{j-N+1}
c_{j-n}
c_{j-n+1}
c_{j-1}
c_j
D
D
D
220
221-N
221-n
221-1
b_N
b_n
b_1
t_j
222

FIG. 3

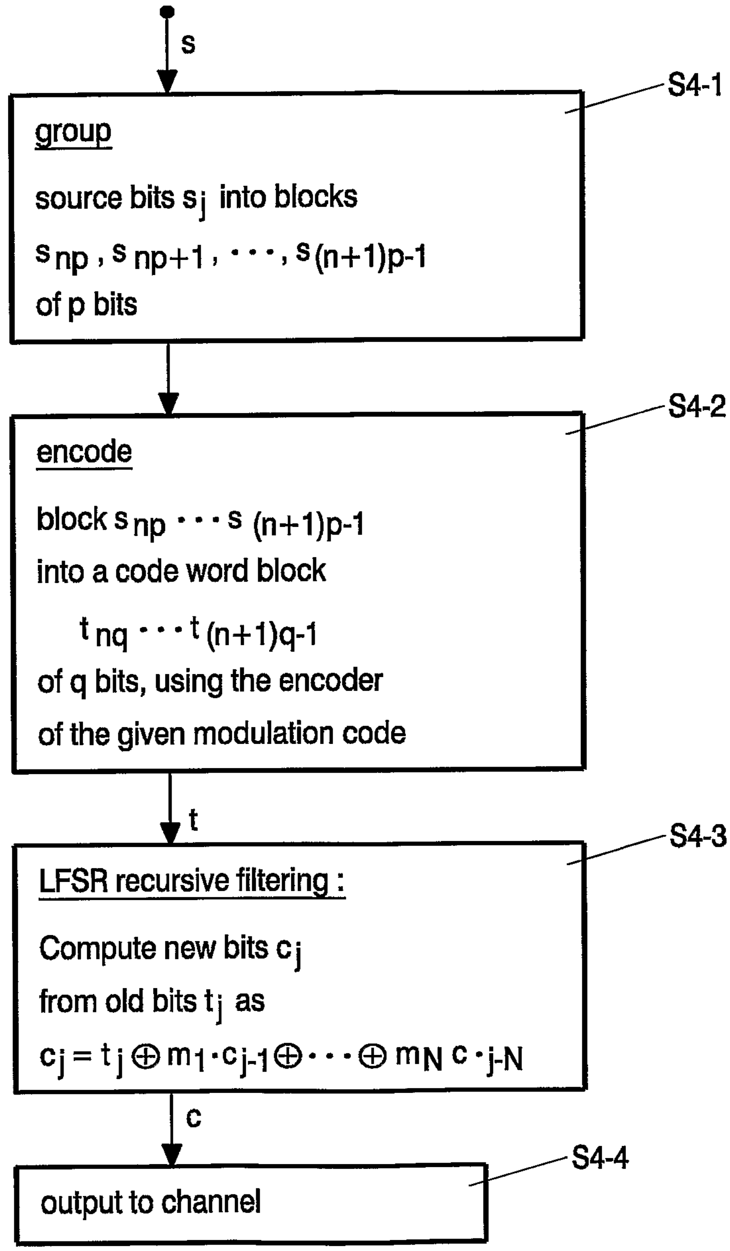

s
S4-1
group
source bits s_j into blocks
$s_{np}, s_{np+1}, \cdots, s_{(n+1)p-1}$
of p bits
S4-2
encode
block $s_{np} \cdots s_{(n+1)p-1}$
into a code word block
$t_{nq} \cdots t_{(n+1)q-1}$
of q bits, using the encoder
of the given modulation code
t
S4-3
LFSR recursive filtering :
Compute new bits c_j
from old bits t_j as
$c_j = t_j \oplus m_1 \cdot c_{j-1} \oplus \cdots \oplus m_N \, c \cdot_{j-N}$
c
S4-4
output to channel

FIG. 4

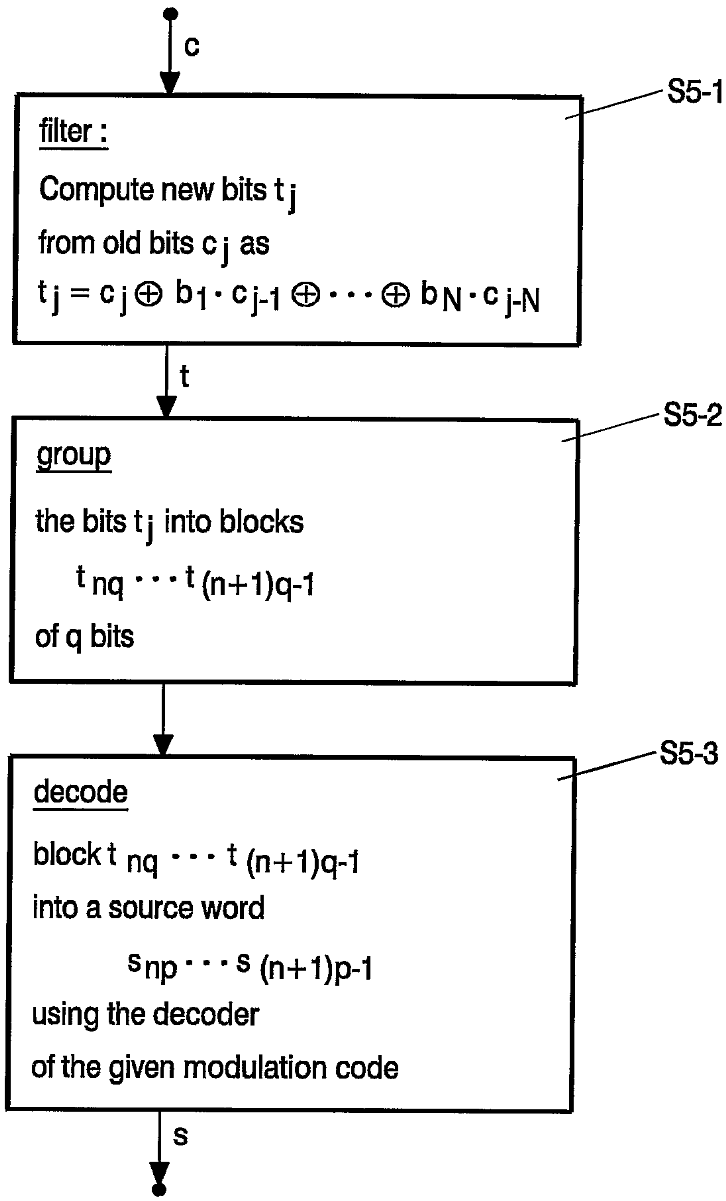

c
S5-1
filter :
Compute new bits t_j
from old bits c_j as
$t_j = c_j \oplus b_1 \cdot c_{j-1} \oplus \cdots \oplus b_N \cdot c_{j-N}$
t
S5-2
group
the bits t_j into blocks
$t_{nq} \cdots t_{(n+1)q-1}$
of q bits
S5-3
decode
block $t_{nq} \cdots t_{(n+1)q-1}$
into a source word
$s_{np} \cdots s_{(n+1)p-1}$
using the decoder
of the given modulation code
s

FIG. 5

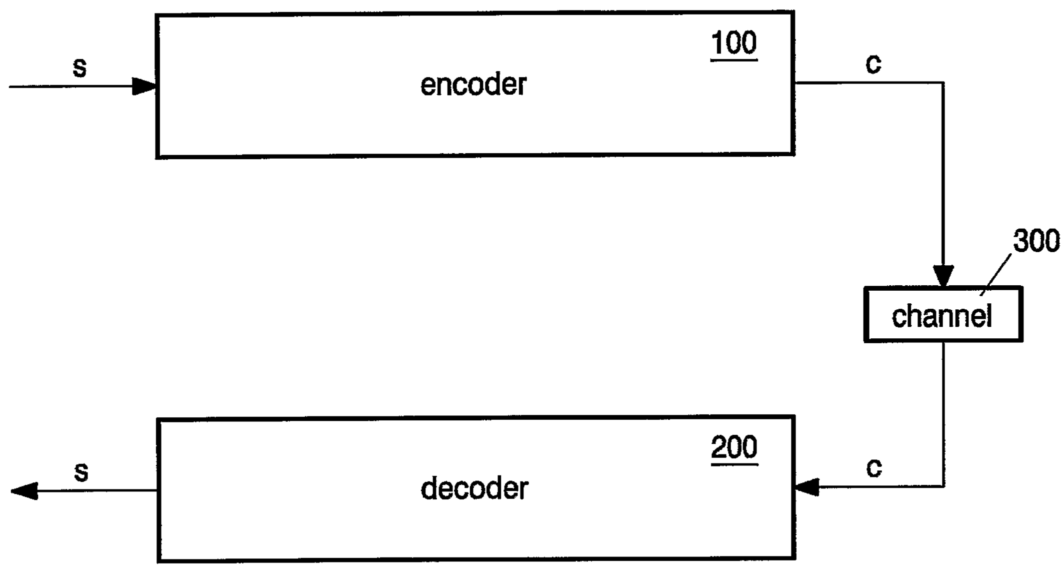


FIG. 6
prior art

PCT/IB2005/051097